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13. ABSTRACT *(Maximum 200 words)*

This final report summarizes the research results obtained with support from ARO for the grant DAAL-90-G-0063 (27076-EL). In this project, we studied approaches for high-speed and low-power recursive and adaptive digital filtering and coding and design methodologies and synthesis for high-performance digital signal processing (DSP) systems.

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Concurrent Architectures for VLSI Signal and Image Processing

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1. Introduction

This final report summarizes the research results obtained with support from ARO for the grant DAAL-90-G-0063 (27076-EL). In this project, we studied approaches for high-speed and low-power recursive and adaptive digital filtering and coding and design methodologies and synthesis for high-performance digital signal processing (DSP) systems. The publications which resulted from this grant [1]-[46] are arranged as book/chapters, journal publications, and conference publications.

2. Pipelined Recursive Digital Filtering

The feedback loop in recursive computations leads to the pipelining bottleneck. To break the bottleneck, we had proposed the *look-ahead* technique. The problems of look-ahead are two fold. First it requires increase in hardware overhead, and second, it leads to inexact pole-zero cancellation in a finite word length implementation. To investigate the degradation due to the second effect, we carried out a thorough finite word length analysis in pipelined recursive digital filters [7][25]. We concluded that at most one or two bits of increase in word length is needed to account for the inexact pole zero cancellation.

To reduce the hardware overhead, we adopted the *constrained filter design* approach. Instead of taking a sequential filter transfer function and pipeline it with look ahead, we addressed the problem of filter design from spectrum specifications with pipelining level as a constraint [14][33]. This approach not only reduced the hardware overhead but also eliminated the inexact pole zero cancellation. This is because during synthesis we can place zeros on unit circle to reduce the hardware cost. We demonstrated that basic, normalized, and scaled normalized lattice digital filters can also be pipelined and can be designed using the constrained filter design method [14][33]. In addition, we showed that the a known lattice filter structure can be derived by scaling another known structure [18][40]. These two previously known structures were derived using different approaches and their relation had not been established.

3. Coder Architectures

We demonstrated that a number of coders including Viterbi and Huffman decoders and source coders containing quantizer loops can be pipelined using the look-ahead technique in spite of the recursive feedback bottleneck [2][6][8][10][22][24][26][31].

4. Adaptive Digital Filters

We proposed a new method referred to as *relaxed look-ahead* to pipeline adaptive digital filters [1]. We proposed three forms of relaxation referred to as *sum, product,* and *delay* relaxations. Using these, we pipelined the least-mean-square (LMS) adaptive digital filter [13][32][35], the adaptive lattice digital filter [12][36][37], the adaptive differential vector quantizer [11][38][42], Kalman filter [20][46], the decision feedback equalizer [21][44], and the adaptive quantizers [45]. We also carried out the detailed finite word length analysis of the adaptive differential pulse code modulation coder using a pipelined LMS adaptive digital filter as its predictor [16][41] and implemented an integrated circuit chip for a video codec in 1.2 micron CMOS technology to demonstrate the impact of the relaxed look-ahead pipelined adaptive filters [4]. While presenting the paper based on this chip [4], we found that Hitachi (Japan) also presented a magnetic recording chip which used an almost identical adaptive filtering algorithm - this clearly shows the usefulness of our proposed adaptive filtering algorithm.

5. Design Methodologies and High Level Synthesis

We proposed a systematic *unfolding technique* to unfold bit-serial systems to digit-serial systems [5][23][27]. Furthermore, we also proposed a reverse *folding* technique to design hardware architectures for time-multiplexed DSP circuits [9][28]. These methodologies and loop scheduling and allocation were used to perform high-level synthesis of DSP systems for time-constrained and resource constrained systems using the Minnesota ARchitecture Synthesis (MARS) system [3][17][19][29] [34]. In addition, we proposed *life time analysis* to minimize the number of registers [30].

6. Tutorial Papers

We also wrote tutorial articles using the results of this project and other projects supported by NSF and ONR [15][39][43].

7. Academic Staff

In addition to the Principal Investigator, three students have been supported from this grant. Jin-Gyun Chung contributed to the recursive digital filtering problems. Since this grant has expired, Mr. Chung is now being supported by NSF and he is expected to complete his Ph.D. in summer 1994. Dr. Naresh Shanbhag contributed to relaxed look-ahead pipelined adaptive digital filter design. He completed his Ph.D. in summer 1993 and is now with AT&T Bell Laboratories in Murray Hill (NJ). Dr. Ching-Yi Wang worked on high-level synthesis and design methodologies. He was partially supported by this grant and partially supported by ONR. He is now my research associate.

8. Papers Published with ARO Grant Support

Books and Book Chapters

(1) N.R. Shanbhag, and K.K. Parhi, *Pipelined Adaptive Digital Filters*, Kluwer Academic Publishers, 1994

(2) K.K. Parhi, "Parallel Processing and Pipelining in Huffman Decoder", (Chapter 12) in *VLSI Implementations for Image Communications*, Series Advances in Image Communications (Edited by Peter Pirsch), **Vol. 2**, Elsevier Science Publisher, Amsterdam, 1993, pp. 365-395

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(16) N.R. Shanbhag, and K.K. Parhi, "Finite Precision Analysis of the ADPCM Coder", *IEEE Transactions on Circuits and Systems-Part II: Analog and Digital Signal Processing*, (accepted October 1993)

(17) C.-Y. Wang, and K.K. Parhi, "High-Level DSP Synthesis using Concurrent Transformations, Scheduling, and Allocation", *Submitted to IEEE Transactions on Computer Aided Design*, July 1992 (Revised June 1993)

(18) J.-G. Chung, and K.K. Parhi, "The Scaled Normalized Lattice Digital Filter", *Submitted to the IEEE Transactions on Circuits and Systems*, October 1992

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